CLAIMS

1. A Digital Subscriber Line [DSL] telecommunication device with a first path for transferring data in a first direction and a second path for transferring data in a second direction opposite to said first direction, said telecommunication device including a plurality of processors (P1 – P4) interconnected with a plurality of memories (M1 – M6),

characterized in that said plurality of processors (P1 – P4) and said plurality of memories (M1 – M6) are respectively arranged as an input/output border column and an input/output border row of an interconnecting matrix architecture, said matrix architecture being constituted by a plurality of interconnection devices (I_{11} – I_{46}) adapted to interconnect the processors of said column with the memories of said row.

2. The Digital Subscriber Line telecommunication device according to claim 1, *characterized in that* said telecommunication device further includes control circuits adapted to control said interconnection devices (I_{11} – I_{46}) for establishing and releasing connections between predetermined processors (P1 – P4) and predetermined memories (M1 – M6).

3. The Digital Subscriber Line telecommunication device according to claim 2, *characterized in that* said control circuits are further adapted to control said interconnection devices (I_{11} – I_{46}) to establish either read access or write access or both to said memories.

4. The Digital Subscriber Line telecommunication device according to claim 1, *characterized in that* each interconnection device of said plurality of interconnection devices is adapted to connect a

particular processor of said plurality of processors with a particular memory of said plurality of memories.

5. The Digital Subscriber Line telecommunication device according to claim 1, characterized in that said first path is a downstream path and in that said second path is an upstream path.

6. The Digital Subscriber Line telecommunication device according to claim 1, characterized in that said telecommunication device operates according to the Very High Speed Digital Subscriber Line [VDSL] protocol.

7. A method for optimizing the transfer of data between memories (M1 – M6) and processors (P1 – P4) of a Digital Subscriber Line [DSL] telecommunication device,

characterized in that said memories (M1 – M6) are shared by said processors (P1 – P4), each processor being able to read data from or to write data to any of said memories under control of control circuits.

8. The method according to claim 7, *characterized in that* a processor may simultaneously access one or more memories during a same predetermined period of time (t3, t4).

9. The method according to claim 8, *characterized in that*, when during a said period of time (t3) a first processor (P1) needs to access a first memory (M2) already accessed by a second processor (P2) during said period of time (t3), the access of said first processor is delayed until a next period of time (t4).

10. The method according to claim 8, *characterized in that* a predetermined number of successive periods of time (t1 · t4) are arranged in a frame (T1, T2, T3), *and in that* said frame is cyclically repeated.